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PATENT **01AB077/ALBRP228US**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant(s): Mark Flood, *et al.*

Serial No: 09/862,941

Filing Date: May 22, 2001

Examiner: Kyung H. Shin

Art Unit: 2143

Title: APPARATUS FOR MULTI-CHASSIS CONFIGURABLE TIME SYNCHRONIZATION

Mail Stop Appeal Brief - Patents
Commissioner for Patents
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APPEAL BRIEF

Dear Sir:

Appellants' representative submits this brief in connection with an appeal of the above identified application. A credit card payment form is filed concurrently herewith in connection with all fees due regarding this appeal brief. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [ALBRP228US].

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I. Real Party in Interest (37 C.F.R. §41.37(c)(1)(i))

The real party in interest in the present appeal is Rockwell Technologies, L.L.C., the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. § 41.37(c)(1)(ii))

Appellant, appellants' legal representatives, and/or the assignee of the present application are unaware of any appeals or interferences which will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. § 41.37(c)(1)(iii))

Claims 1-52 stand rejected by the Examiner. The rejection of claims 1-52 is being appealed.

IV. Status of Amendments (37 C.F.R. § 41.37(c)(1)(iv))

Claims 3-34, and 36-52 were amended to correct minor informalities and those claim amendments have been entered after the Final Office Action.

V. Summary of Claimed Subject Matter (37 C.F.R. § 41.37(c)(1)(v))

A. Independent Claim 1

Independent claim 1 recites a time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising: a processor interface for interfacing the synchronization apparatus with a host processor; a transmitter adapted to transmit synchronization information and data to a network in the control system; a receiver adapted to receive synchronization information and data from the network; and a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor. (*See e.g.*, page 9, lines 18-26; page 10, lines 10-36; page 38, lines 24-29; FIGS. 1, 2, 33, 34).

B. Independent Claim 38

Independent claim 38 recites a synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller outside the control chassis, comprising: a host processor in communication with the first controller via a backplane bus in the control chassis; a transmitter adapted to transmit synchronization information and data to a network in the control system; a receiver adapted to receive synchronization information and data from the network; a timing system including a clock that maintains an indication of time according to information received from one of the network and the host processor; and a synchronization circuit operatively associated with the host processor, the transmitter, the receiver, and the timing system, and configurable by the host processor to operate the module as one of a synchronization master and a synchronization slave. (*See e.g.*, page 9, lines 18-26; page 10, lines 10-36; page 38, lines 9-29; FIGS. 1, 2, 33, 34).

C. Independent Claim 39

Independent claim 39 recites a synchronization circuit for synchronizing operation of a first controller with that of a second controller in a control system, comprising: a processor interface for interfacing the synchronization circuit with a host processor; a transmitter component adapted to transmit synchronization information and data to a network in the control system; a receiver component adapted to receive synchronization information and data from the network; and a timing system including a clock that maintains an indication of time according to information received from one of the network and the host processor, the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave. (*See e.g.*, page 9, lines 18-26; page 10, lines 10-36; page 38, lines 9-29; FIGS. 1, 2, 33, 34).

C. Independent Claim 52

Independent claim 52 recites a synchronization system for synchronizing a first controller with a second controller in a control system, comprising: means for interfacing the synchronization circuit with a host processor (*see e.g.*, page 9, line 27-page 10, line 26; page 11, line 27-page 12, line 4; page 38, line 9-page 41, line 6; FIGS. 1, 2, 33, 34); means for transmitting synchronization information and data to a network in the control system (*see e.g.*, page 26, line 27-page 32, line 10; FIGS. 1, 2, 10, 11, 33, 34); means for receiving synchronization information and data from the network (*see e.g.*, page 26, line 27-page 32, line 10; FIGS. 1, 2, 10, 11, 33, 34); and means for maintaining an indication of time according to information received from one of the network and the host processor, the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave (*see e.g.*, page 37, lines 6-15; page 39, lines 1-18; FIGS. 1, 2, 10, 11, 33, 34).

VI. Grounds of Rejection to be Reviewed (37 C.F.R. § 41.37(c)(1)(vi))

A. Whether claims 1-7, 13-28, 30-34, 38-46 and 48-52 are unpatentable under 35 U.S.C. §102(e) over Voth (US 6,199,169).

B. Whether claims 8-12 are unpatentable under 35 U.S.C. §103(a) over Voth (US 6,199,169) in view of Ramussen, *et al.* (US 6,449,732).

C. Whether claims 8-12 are unpatentable under 35 U.S.C. §103(a) over Voth (US 6,199,169) in view of Kuribayashi, *et al.* (US 6,775,246).

VII. Argument (37 C.F.R. § 41.37(c)(1)(vii))

A. Rejection of Claims 11-7, 13-28, 30-34, 38-46 and 48-52 Under 35 U.S.C. §102(e)

Claims 1-7, 13-28, 30-34, 38-46 and 48-52 stand rejected under 35 U.S.C. §102(e) as being unpatentable over Voth (US 6,199,169). It is respectfully submitted that this rejection

should be reversed for at least the following reasons. Voth does not teach or suggest all features of the subject claims.

> A <u>**single**</u> prior art reference anticipates a patent claim only if it expressly or inherently describes ***each and every limitation set forth in the patent claim***. *Trintec Industries, Inc., v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 U.S.P.Q.2D 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987) (emphasis added). ***The identical invention must be shown in as complete detail as is contained in the ... claim***. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

Appellants' claimed subject matter relates generally to industrial control systems with a time synchronization apparatus for synchronizing operation of a first controller with that of a second controller. More specifically, the claimed subject matter discloses a system comprising distinct components, each with explicit structural interrelationships with other components: 1) either a processor interface or a backplane bus in a control chassis, 2) a synchronization apparatus, 3) a host processor, 4) a network in the control system, and 5) a second controller. For example, the synchronization apparatus comprises a processor interface, and the host processor is structurally interrelated with the synchronization apparatus by a processor interface (or a backplane bus as in claim 38). Similarly, the host processor is structurally interrelated with the second controller by a network in the control system. Moreover, the processor interface (or backplane bus) is distinct from the network in the control system because the former is a structural interface between a synchronization apparatus and a host processor, while the latter is a structural interface between the host processor and the second processor. In particular, independent claim 1 (and similarly independent claims 38 and 39) recites, "a ***second controller*** ... a ***processor interface*** for interfacing the ***synchronization apparatus*** with a ***host processor*** ... and ... a ***network*** in the control system". Additionally, independent claim 1 (and similarly independent claims 38, 39 and 52) recites, "a transmitter adapted to transmit *synchronization information and* ***data*** to a ***network in the control system***". Voth does not teach or suggest these novel features.

Rather, Voth relates to a method of time synchronization in a computer cluster system. (*See* Abstract). The system includes a master node and a plurality of slave nodes, interconnected *via* a computer network (*see* FIG. 1; col. 4, ll. 7-17), and employs native operating system commands to affect time synchronization between the nodes (*see* col. 4, ll. 64-67; FIG. 4; *e.g.*, the SYNC and INFO commands represent the operating system commands). Accordingly, the master node cannot be both the synchronization apparatus and the host processor because the subject claims recite "the synchronization apparatus" interfaces "with a host processor" *via* "a processor interface." Further, at page 2 of the Final Office Action (dated June 30, 2005), the Examiner indicates that the Voth's network 104 is a processor interface, however, Voth's master node does not comprise the network 104. Hence, the master node of Voth does not interface with itself, and even were it to do so, then Voth does not teach ***a processor interface*** for interfacing the synchronization apparatus with a host processor.

In order to circumvent these apparent deficiencies with the reference, the Examiner incorrectly reasons that the system (*e.g.*, system 100 of FIG. 1) is the synchronization apparatus (*see* Final Office Action, page 2; "Voth discloses a system (*i.e.*, an apparatus) capable of performing a particular single purpose, which is time synchronization"). Under this rationale, the system comprises a processor interface (*e.g.*, network 104) but also comprises the master node and the slave nodes. Therefore, the nodes are internal constituents of the system and may be interfaced with one another, but are not interfaced to the system. That is, while the system may *contain* a host processor, it does not *interface* with a host processor. Thus, Voth does not teach or suggest a processor interface ***for interfacing the synchronization apparatus with a host processor***. Voth does not teach or suggest that the system is interfaced with anything, let alone a host processor.

The Examiner tacitly ignores this shortcoming by citing a single component in Voth to represent multiple distinct components of the subject claims, even though by doing so, the Examiner has destroyed the claimed structural interrelationship between the distinct components. For example, the Examiner suggests that Voth's master node 102a is a host processor, any one of the slave nodes 102b-d is a second controller in a control system, and the network 104 is both a network in the control system and a processor interface (or a backplane bus) included in the synchronization apparatus. Simultaneously, it is the Examiner's position that the entire system is the synchronization apparatus, even though the system contains the master node, whereas the

synchronization apparatus does not include the host processor (master node), but rather is interfaced with the host processor.

In essence, the Examiner is taking each component in isolation, and then citing a component from Voth that, in isolation, can be characterized as similar, but entirely without regard to the claimed interrelationships with the other components. For example, if, as the Examiner alleges, the system 100 is a synchronization apparatus, then Voth does not teach or suggest, nor does the Examiner argue, that they system 100 is interfaced with anything, let alone a host processor. Rather, the Examiner relies on a showing that the system 100 contains a host processor (*e.g.*, the master node), not that the system 100 is interfaced to a host processor. Moreover, Voth teaches that the network 104 interfaces the master node 102a to slave nodes, but the Examiner alleges that the network 104 is both the network in the control system as well as the processor interface contained in the synchronization apparatus even though such dual representation by the network 104 is mutually exclusive. The synchronization apparatus comprises the ***processor interface*** and *a transmitter adapted to transmit synchronization information and data to* ***a network in the control system***, but it does not comprise the network in the control system. Therefore, the network 104 cannot be both the processor interface (that is contained in the synchronization apparatus) and network in the control system (that is remote from the synchronization apparatus). Accordingly, Voth does not disclose the identical invention in as complete detail as in the subject claims, and this rejection should be reversed.

Appellants' claimed subject matter also relates to a synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller ***outside the control chassis***. In particular, independent claim 38 recites, "A synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller ***outside the control chassis***, comprising: a host processor in communication with the first controller ***via a backplane bus in the control chassis***; a transmitter adapted to transmit synchronization information and data to ***a network in the control system***". Voth does not teach or suggest each and every feature of the subject claim.

In particular, Voth teaches only a means by which the constituents of the system 100 can communicate with other constituents, *i.e.*, the network 104, whereas the instant claims recites distinct components with distinct structural interrelationships by which communication is possible (*e.g.*, a backplane bus and a network in the control system). The Examiner indicates

that the network 104 is the backplane bus in the control chassis. (*See* Final Office Action, page 9). Therefore, Voth does not teach or suggest transmitting synchronization information and data to ***a network in the control system***. Voth is silent as to whether the network 104 (*i.e.*, the backplane bus in the control chassis) can communicate with anything outside of the system 100, let alone a second controller ***outside the control chassis***.

Appellants' claimed subject matter further relates to a synchronization circuit for synchronizing operation of a first controller with that of a second controller in a control system. In particular, independent claim 39 (and similarly independent claim 52) recites, "the synchronization circuit is ***configurable by the host processor*** to operate as one of a synchronization master and a synchronization slave." Voth does not teach or suggest these novel features. Rather, Voth teaches that one of the nodes assumes a master role and the remaining nodes function as slaves (*see* col. 4, ll. 37-39), but the reference is silent regarding whether the nodes are *configurable by the host processor*. Accordingly, Voth does not teach or suggest the synchronization circuit is ***configurable by the host processor*** to operate as one of a synchronization master and a synchronization slave.

Moreover, independent claim 1 (and similarly independent claims 38, 39 and 52) recites, "a transmitter adapted to transmit *synchronization information and* ***data*** to a network in the control system", whereas Voth discloses a system to transmit synchronization information, but not synchronization information and data. At page 3 of the Final Office Action, the Examiner concedes that the reference does not disclose these claim limitations, but introduces a secondary reference the Examiner alleges cures this deficiency (*i.e.*, "*Voth in view of Kuribayashi discloses the capability to transmit time synchronization information and non time synchronization data over an interconnected network*"). In order to maintain this rejection, the Examiner must establish that the teachings found in Kuribayashi are inherent described in Voth, but the Examiner has not made such a demonstration.

> "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950 (Fed. Cir. 1999) (*quoting Continental Can co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991)). ***"Inherency, however, may not be***

> ***established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.*** " *Mehl/Biophile Int'l Corp. v. Milgraum*, 192 F.3d 1362, 1365, 52 USPQ2d 1303, 1305 (Fed. Cir. 1999), reh'g denied, 1999 U.S. App. LEXIS 31386 (Fed. Cir. Oct. 27, 1999) (*quoting In re Oelrich*, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981)).

The Examiner has not even suggested that the indicated teachings of Kuribayashi are inherent in Voth let alone attempted to incorporate this suggestion in her arguments. Rather, the Examiner points out "Voth discloses a system that is capable of performing a particular single purpose, which is time synchronization." (*See* Final Office Action, page 2). Accordingly, Voth does not teach or suggest the capability to transmit synchronization information and data such as *e.g.*, control data described in the specification portion of appellants' disclosure at *e.g.*, page 19, line 12. In contrast, Voth teaches a particular, single type of information transmitted, which is time synchronization information. Pursuant to *Milgaum*, inherence may not be established by possibilities...the mere fact that the system disclosed in Voth may transmit data as well as time synchronization information is not sufficient to establish inherency.

Accordingly, the Examiner has relied upon the teachings of more than a single reference to rejection the subject claims, but has not shown or even declared that the secondary reference was employed to show inherency. In view of at least the above, it is apparent Voth does not disclose or suggest the claimed subject matter as described in independent claims 1, 38, 39 and 52 as well as the associated dependent claims. Accordingly, this rejection should be reversed.

B. Rejection of Claims 8-12 Under 35 U.S.C. §103(a)

Claims 8-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Voth (US Patent No. 6,199,169) in view of Ramussen, *et al.* (US Patent No. 6,449,732). Reversal of this rejection is respectfully requested because Voth and Ramussen, *et al.*, either alone or in combination, fail to teach or suggest the appellants' claimed subject matter. In addition, Voth is directed toward non-analogous art and is therefore not reasonably pertinent to be relied upon as a basis for rejection.

Claims 8-12 depend directly or indirectly upon independent claim 1. As noted *supra*, Voth does not teach or suggest the claimed subject matter. Ramussen, *et al.* fails to make up for the aforementioned deficiencies of Voth and this rejection should be reversed. Moreover, Voth

is non-analogous art. "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 144, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). See also *In Re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986); *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992). Voth relates to a method of synchronization, however, this method employs software rather than hardware and is very limited because it works in a Single System Image (SSI) computer cluster (*see* col. 4, ll. 35-38) that requires a very high speed network (*see* col. 4, ll. 19-22), whereas the claimed subject matter recites a synchronization apparatus/circuitry for use with industrial controllers in a distributed control system network. For example, in Voth, the maximum round-trip time of a SYNC message sent from the master to the slave and back to the master is assumed to be no more than 1 microsecond (*i.e.*, 1μs). (*See* col. 8, ll. 44-56). While this round-trip time of 1μs is exemplary, and other values are contemplated (up to 5μs; *see* col. 8, ll. 64-66), the precision of the synchronization algorithm is proportionate to the speed of the network. (*See* col. 8, ll. 57-58).

In order to affect synchronization, the round-trip time for a SYNC message must be less than half of a clock tick, where a clock tick is taught to be 10μs. (*See* col. 8, ll. 60-66). The synchronization algorithm effectively treats the propagation time (*i.e.*, latency) between the nodes as zero when synchronizing, which is why the round-trip time must be extremely fast or about 1μs, and also why this method applies only to SSI computer clusters or similar systems with very high speed networks of a particular topology. The reference will not work in conventional networks in a control system or with controllers that communicate with other controllers outside the time zone or outside the first control chassis. For Example, the latency between the controllers can be on the order of 50μs (producing a 100μs round-trip time), which is about 20 times too imprecise to affect synchronization using the method disclosed in Voth. Moreover, Voth cannot function in topologies other than a star topology wherein all slave nodes are directly connected to the master node, whereas conventional networks in a control system assume many topologies, such as a daisy-chain and ring topologies. In various other topologies, the round-trip time to communicate from the master to all slave nodes and back can be on the order of 1200 milliseconds, which is about 240,000 times too imprecise to affect synchronization

by employing the method of Voth. Moreover, Voth relies upon inherent operating system calls such as the UNIX SYNC message, whereas typical controllers in a control system are not installed with full-service operating systems intended for commercial use. As such, Voth cannot function within conventional industrial control system network environments, and is therefore not "reasonably pertinent to the particular problem with which the inventor was concerned."

C. **Rejection of Claims 29, 35-37 and 47 Under 35 U.S.C. §103(a)**

Claims 29, 35-37 and 47 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Voth (US Patent No. 6,199,169) in view of Kuribayashi, *et al.* (US Patent No. 6,775,246). Reversal of the rejection is respectfully requested for at least the following reasons. Voth and Kuribayashi, *et al.*, alone or in combination, do not teach or suggest the appellants' claimed subject matter. Voth relates to non-analogous art and cannot be relied upon as a basis for rejection.

Claims 29 and 35-37 depend directly or indirectly upon independent claim 1 while claim 47 depends directly or indirectly upon independent claim 39. As noted *supra*, Voth fails to teach or suggest appellants' claimed subject matter as recited in the subject claims. Kuribayashi, *et al.* fails to make up for the aforementioned deficiencies of Voth with respect to independent claims from which claims 29, 35-37 and 47 depend, respectively. Moreover, as submitted *supra* with respect to the rejection of claims 8-12, Voth is non-analogous art, and as such cannot be used as a basis for rejection. Accordingly, this rejection should be reversed.

In addition, independent claim 35 recites, the time synchronization apparatus of claim 1, being configured as an intermediate node in a ***daisy-chain topology***, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain. Neither Voth nor Kuribayashi, *et al.* teach or suggest a daisy-chain topology. The examiner alleges that Kuribayashi, *et al.* teaches a daisy-chain topology, yet neither the indicated portions nor anywhere else does the reference teach this aspect. Moreover, the method disclosed in Voth relies on direct and nearly instantaneous communication between the nodes in order to affect time synchronization because the method treats the round-trip time of communication between the nodes as zero. Therefore, even if Kuribayashi, *et al.* did teach a daisy-chain topology, the combination of a daisy-chain topology from Kuribayashi, *et al.* would render the

time synchronization method disclosed in Voth inoperable because at least one clock cycle would be required to assert an instruction to forward the SYNC message to another node (and more clock cycles for each node connected along the daisy-chain), thereby effectively guaranteeing that all round-trip times will exceed the maximum allowable value (*i.e.*, one-half of a clock cycle) and be rejected, terminating the method without any synchronization occurring. (*See* col. 6, ll. 50-55).

D. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 1-52 be reversed.

If any additional fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [ALBRP228US].

Respectfully submitted,
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VIII. Claims Appendix (37 C.F.R. § 41.37(c)(1)(viii))

1. A time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising:

a processor interface for interfacing the synchronization apparatus with a host processor;

a transmitter adapted to transmit synchronization information and data to a network in the control system;

a receiver adapted to receive synchronization information and data from the network; and

a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor.

2. The time synchronization apparatus of claim 1, being configurable to operate as one of a synchronization master and a synchronization slave.

3. The time synchronization apparatus of claim 1, being configured to operate as a synchronization master, the transmitter periodically transmits message frames at a fixed period.

4. The time synchronization apparatus of claim 3, the fixed period is about 50μs.

5. The time synchronization apparatus of claim 3, the transmitter transmits a message frame having an LCM indicator at a least common multiple (LCM) interval.

6. The time synchronization apparatus of claim 5, the LCM interval is 600ms.

7. The time synchronization apparatus of claim 3, being configured as a synchronization master, the transmitter transmits message frames having multiplexed data and direct data.

8. The time synchronization apparatus of claim 7, the frame comprises three flag bytes, a control byte, a data field comprising the multiplexed data and the direct data, and two CRC bytes.

9. The time synchronization apparatus of claim 8, the data field comprises 6 32 bit words, and the amount of multiplexed data and the amount of direct data in each message frame is configurable.

10. The time synchronization apparatus of claim 9, each message frame comprises a direct data portion and a multiplexed data portion, the direct data comprises the direct data portion of a single frame, and the multiplexed data comprises the multiplexed data portions of a plurality of frames.

11. The time synchronization apparatus of claim 10, the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame.

12. The time synchronization apparatus of claim 9, the amount of multiplexed data and the amount of direct data in each message frame is configurable according to information from the host processor.

13. The time synchronization apparatus of claim 7, the timing system is adjustable according to information received from the host processor.

14. The time synchronization apparatus of claim 1, being configured as a synchronization slave, the receiver receives message frames at a fixed period, and the timing system is adjusted according to the fixed period.

15. The time synchronization apparatus of claim 14, the fixed period is about 50μs.

16. The time synchronization apparatus of claim 14, the receiver receives a message frame having an LCM indicator at a least common multiple (LCM) interval.

17. The time synchronization apparatus of claim 16, the LCM interval is 600ms.

18. The time synchronization apparatus of claim 16, the timing system is adjusted according to the LCM indicator.

19. The time synchronization apparatus of claim 16, the receiver interrupts the host processor according to the LCM indicator.

20. The time synchronization apparatus of claim 14, the transmitter transmits message frames at the fixed period.

21. The time synchronization apparatus of claim 20, the message frames received and transmitted by the receiver and transmitter, respectively, comprise multiplexed data and direct data.

22. The time synchronization apparatus of claim 21, the message frames comprise a data field with 6 32 bit words, and the amount of multiplexed data and the amount of direct data in each message frame is configurable.

23. The time synchronization apparatus of claim 22, each message frame comprises a direct data portion and a multiplexed data portion, the direct data comprises the direct data portion of a single frame, and the multiplexed data comprises the multiplexed data portions of a plurality of frames.

24. The time synchronization apparatus of claim 23, the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame.

25. The time synchronization apparatus of claim 24, the receiver presents direct data from received message frames to the host processor at the fixed period.

26. The time synchronization apparatus of claim 25, the receiver presents multiplexed data from received message frames to the host processor at a multiple of the fixed period.

27. The time synchronization apparatus of claim 14, comprising a multiplier receiving an operand from the receiver, a multiplication value from the host processor, and providing a multiplication result value to at least one of the host processor and the transmitter, the multiplication result value is the product of the multiplication value and the operand.

28. The time synchronization apparatus of claim 27, the direct data received in the message frame comprises the operand.

29. The time synchronization apparatus of claim 14, the message frame comprises a status component indicative of the status of an upstream device, the receiver provides the status component to the host processor.

30. The time synchronization apparatus of claim 14, the transmitter transmits message frames at the fixed period comprising direct data and multiplexed data.

31. The time synchronization apparatus of claim 30, at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, the direct data from a received message frame is passed through to the transmitter.

32. The time synchronization apparatus of claim 30, comprising a multiplier, at least a portion of the direct data in the message frames transmitted by the transmitter comprises a multiplication result value provided to the transmitter by the multiplier.

33. The time synchronization apparatus of claim 30, at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the host processor.

34. The time synchronization apparatus of claim 33, the multiplexed data in the message frames transmitted by the transmitter is provided to the transmitter by the host processor.

35. The time synchronization apparatus of claim 1, being configured as an intermediate node in a daisy-chain topology, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain.

36. The time synchronization apparatus of claim 35, the receiver receives message frames at a fixed period, and the transmitter transmits message frames at the fixed period comprising direct data and multiplexed data.

37 The time synchronization apparatus of claim 36, at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, the direct data from a received message frame is passed through to the transmitter.

38. A synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller outside the control chassis, comprising:

a host processor in communication with the first controller via a backplane bus in the control chassis;

a transmitter adapted to transmit synchrouization information and data to a network in the control system;

a receiver adapted to receive synchronization information and data from the network;

a timing system including a clock that maintains an indication of time according to information received from one of the network and the host processor; and

a synchronization circuit operatively associated with the host processor, the transmitter, the receiver, and the timing system, and configurable by the host processor to operate the module as one of a synchronization master and a synchronization slave.

39. A synchronization circuit for synchronizing operation of a first controller with that of a second controller in a control system, comprising:

a processor interface for interfacing the synchronization circuit with a host processor;

a transmitter component adapted to transmit synchronization information and data to a network in the control system;

a receiver component adapted to receive synchronization information and data from the network; and

a timing system including a clock that maintains an indication of time according to information received from one of the network and the host processor,

the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave.

40. The system of claim 39, the transmitter component periodically transmits message frames comprising direct data, and the direct data is obtained from at least one of the receiver component and the host processor.

41. The system of claim 39, further comprising a multiplier, the transmitter component periodically transmits message frames comprising direct data, and the direct data is obtained from at least one of the receiver, the host processor, and the multiplier.

42. The system of claim 39, the transmitter component periodically transmits message frames comprising multiplexed data, and the multiplexed data is obtained from the host processor.

43. The system of claim 39, the transmitter component periodically transmits message frames comprising direct data and multiplexed data, and the amount of the multiplexed data in the message frames and the amount of direct data in the message frames is configurable.

44. The system of claim 39, the receiver component periodically receives message frames comprising direct data, multiplexed data, and status information from the network, and the synchronization circuit provides at least one of received direct data, received multiplexed data, and received status information from the receiver component to the host processor.

45. The system of claim 44, further comprising a multiplier operating on the received direct data, and the synchronization circuit provides a multiplier result value from the multiplier to the host processor.

46. The system of claim 45, the synchronization circuit provides a multiplication value to the multiplier from the host processor.

47. The system of claim 44, the status information comprises at least one of status of an upstream device, and an error counter.

48. The system of claim 39, the transmitter component periodically transmits message frames comprising direct data, multiplexed data, and configuration information, and the synchronization circuit provides at least one of the direct data, multiplexed data, and configuration information to the transmitter component from the host processor.

49. The system of claim 39, the transmitter component periodically transmits message frames having synchronization information, the synchronization information is obtained from the timing system, and the timing system is adjusted according to at least one of synchronization information received from the network and synchronization information from the host processor.

50. The system of claim 39, the synchronization circuit interrupts the host processor according to receipt of an LCM indicator by the receiver.

51. The system of claim 39, the synchronization circuit interrupts the host processor periodically for presentation of at least one of direct data and multiplexed data from the receiver to the host processor.

52. A synchronization system for synchronizing a first controller with a second controller in a control system, comprising:

means for interfacing the synchronization circuit with a host processor;

means for transmitting synchronization information and data to a network in the control system;

means for receiving synchronization information and data from the network; and

means for maintaining an indication of time according to information received from one of the network and the host processor, the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave.

IX. Evidence Appendix (37 C.F.R. §41.37(c)(1)(ix))

None.

X. Related Proceedings Appendix (37 C.F.R. §41.37(c)(1)(x))

None.